219.40780X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: B. CHANDRAN, et al.

Serial No: 10/023,723

Filed: December 21, 2001

Title: SEMICONDUCTOR PACKAGE WITH LOW RESISTANCE PACKAGE-TO-DIE INTERCONNECT SCHEME FOR REDUCED DIE STRESSES

Group: 2827

Examiner: James M. MITCHELL

AMENDMENT

Assistant Commissioner for Patents
Washington DC 20231

January 30, 2003

Sir:

The following amendments and remarks are submitted in the above-identified application in response to the Office Action mailed November 6, 2002.

IN THE CLAIMS:

Please cancel claims 2, 6, 8, 18, 20 and 23 and amend the claims to read as follows:

1. (Amended) An electronic assembly comprising:

a substrate;

a die;

a plurality of interconnections between the substrate and die;

wherein respective ones of the interconnections include a relatively low melting temperature and yield strength reflowed solder bump on the die, a relatively higher melting temperature and electrically conductive material